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GABOR FILTER USING VEDIC MATHEMATICS

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Abstract- Now a days most of the processors essentially contain multipliers as its base element. Speed of the processors depends on the speed of multiplier. Addition, multiplication and signal delay is necessary to design filters. Sixteen sutras are old fashioned Vedic mathematics, out of them Urdhva Triyakbhyam sutra are observed which is applied for filters. This sutra is mainly used to multiply numbers in crosswise manner, where conventional multiplication takes a excess time to multiply numbers and calculate the product and UT is used improve speed of the processor. The Urdhva Triyabhyam and conventional multiplication techniques are compared in terms of power, time delay and area. This presents the design of multipliers using Urdhva Triyakbhyam and has been coded in Verilog language, it is synthesised and simulated using cadence software.

Keywords – vedic mathematics, Uradhava Triyakbhyam technique, verilog, cadence software.

I. INTRODUCTION

Multiplication plays a fundamental operation in arithmetic. Multiply and accumulate operations are used in many digital signal operations like FFT, DFT, convolution and arithmetic and logic unit of microprocessors. In many DSP applications, the Multiply Accumulate unit is a major contributing factor to the critical path delay and will affect the performance of application. Low values of time delay and power consumption are the major specification for many applications. This paper describes high –speed, area efficient and lower power Vedic multiplier.
The Vedic multiplier is based on the vedic multiplication formulae called Sutras. Urdhva Triyakbhyam Sutra is a general multiplication sutra applicable to all cases of multiplication. The meaning of Urdhva Triyakbhyam is vertically and crosswise. The end digits of two lines are multiplied and the output is summed with the previous carry. Initially the carry-in is taken to be zero. When there are more lines in single step, all the outputs are summed to the previous carry. LSB of the number will one of the final output digits and the rest will act as the carry in for next step.

VEDIC MATHEMATICS

Vedic mathematics is the ancient system of mathematics which has a unique technique for fast mental calculations, based on 16 sutras. This is a different technique all together and is considered very close to the way a human mind works. A large amount of work has so far been done for understanding these sutras. As the mathematical operations using Vedic methods are fast, we can improve the computational speed to perform fast arithmetic operations in the processor. These algorithms simulated in software and converted into dedicated hardware multipliers can be used to design arithmetic unit in DSP processors and numeric co processors. The basic idea is to divide and conquer the large multiplication by exploiting the parallel processing capabilities which are inherent in Very High Speed Integrated Circuit Hardware Description Language (VHDL) .Vedic mathematics is mainly based on 16 sutras which

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deals with various branches of mathematics like arithmetic, algebra, geometry etc., Jagadguru Shankaracharya Bharathi Krishna Teerthaji Maharaja (1884-1960) comprised all this work together and gave its mathematical explanation. After extensive research in Atharva Veda Swamiji constructed 16 sutras and 16 upa sutras. Vedic mathematics deals with several basic as well as complex mathematical operations. The methods of vedic mathematics are extremely simple and very powerful.

The 16 sutras are:

1) (Aunrupye)Shunyamanyat -If one is in ratio, the other is zero.

2) Chalana-kalanabhyam -Differences and similarities

3) Ekadhikina Purvena -By one more than the previous one

4) Ekanyunena Purvena -By one less than the previous one

5) Gunakasamuchyah -The factors of the sum is equal to the sum of factors

6) Gunitasamuchyah -The product of the sum is equal to the sum of the product.

7) Nikhilam Navatashcaramam Dashtah -All from 9 and last from 10

8) Parvarya yojayet -Transpose and adjust.

9) Puranapuranabhyam -By the completion or no completion

10) Sankalana-vyavakalanbhyam –By addition and by subtraction

11) Shesanyankena-Charamena -the remainders by the last digit.

12) Shunyam Saamyasamuccaye -when the sum is the same that sum is zero

13) Sopaantyadvayamantyam -the ultimate and twice the penultimate

14) Urdhva Triyabhyam -vertically and crosswise

15) Vyashtisamansith -part and whole

16) Yaavadunam -whatever the extent

I. PROPOSED ALGORITHM

Vedic multiplier algorithm –

One of the sutra under vedic mathematics is Uradhava Triyakbhyam. UT sutra is a general multiplication formula applicable to all cases of multiplication. It literally means, “Vertical and Crosswise”. The work has proved the efficiency UT vedic method for multiplication which strikes a difference in the actual process of multiplication itself. It enables parallel generation of intermediate products, eliminates unwanted multiplication steps with zeros and scaled to higher bit levels using Karatsuba algorithm with the compatibility to different data types. These Multipliers have an important effect in designing arithmetic, signal and image processors. Many mandatory functions in such processors make use of multipliers. (For example, the basic building blocks in Fourier transforms (FFT’s) and MAC).

A. 2*2 Vedic Multiplication

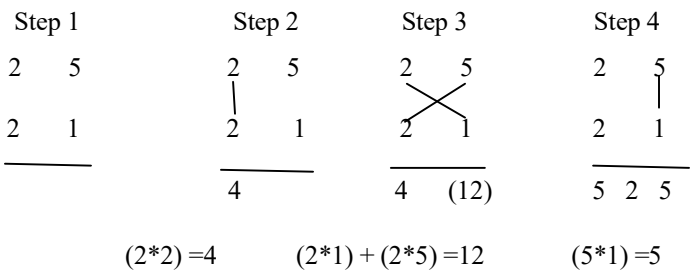

Fig 1: UT technique for 2*2 Multiplication

4*4 Vedic Multiplication

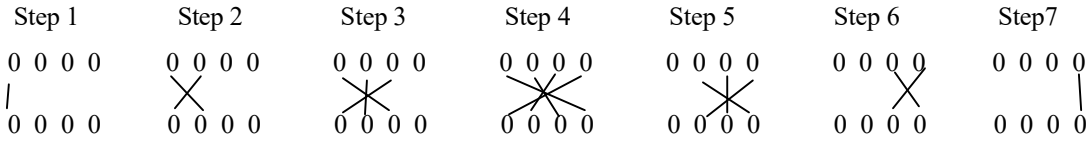

Fig 2: UT technique for 4*4 Multiplication

III. Experiment and Result

The data is analysed in terms of timing power and area using cadence software. The output waveform and the schematic are also obtained. Here the result from the cadence is compared with the results of Xilinx ISE. The input and output waveform for the considered data is as shown in Fig 3 and Fig 4. Here x0-x7 and h0-h7 indicates the input and y0-y14 indicates output.

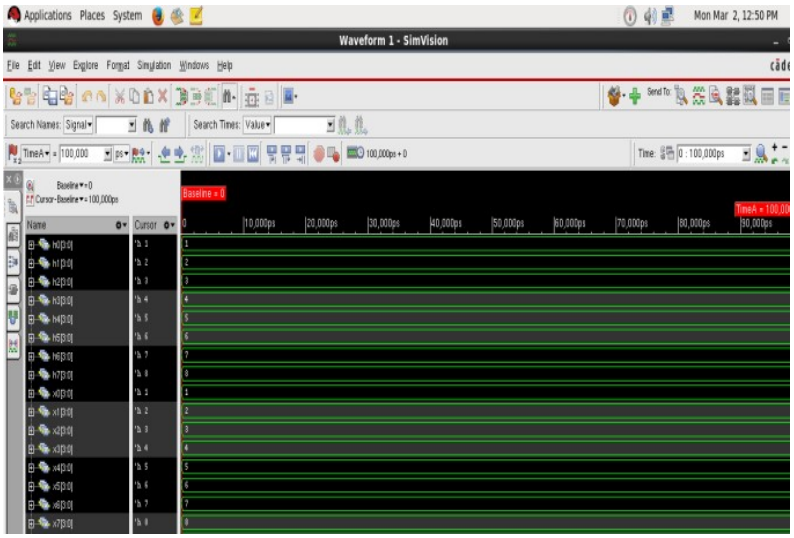

Fig 3: Input waveform

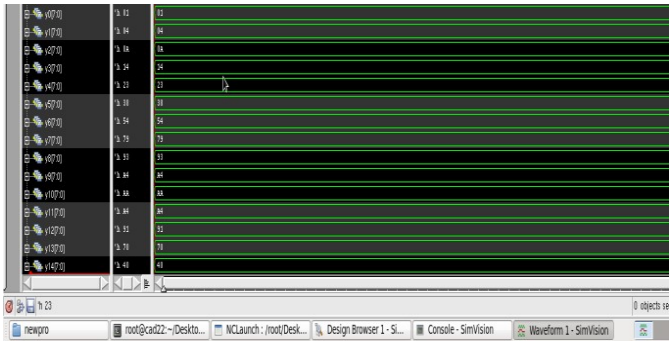

Fig 4: Output waveform

Table -1 Experiment Result

Parameter	Convolution with normal multiplier	Convolution with UT multiplier
Propagation Delay	48.57nss	22.306ns
Power	97mW	81mW

Table 1 show the comparison between the convolution with the normal multiplier and convolution with UT multiplier from the table we can observe that UT multiplier consume less power and and it has less delay when compare to normal multiplier.

IV.CONCLUSION

The proposed Multiplier design using Urdhva-Triyakbhyam sutra of vedic mathematics, being the key component of Arithmetic and Logical Unit, Multiplier and accumulate units, determines the performance and throughput of the applications. Generally, the vedic multipliers are much faster than the conventional multipliers. This gives us scheme for hierarchical multiplier design. So, the design density gets condensed for inputs of large number of bits and modularity gets augmented. Urdhva-Triyakbhyam, Nikhilam and Anurupye sutras are such vedic sutras which can reduce delay, power and hardware requirements for multiplication of numbers. Hence the designed multiplier and the MAC unit for the filters can be used in various applications like digital signal processing, VLSI signal processing, encryption and decryption algorithms in cryptography etc. The proposed design can further be implemented for 16x16, 32x32 multipliers.

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