REDUCTION IN AREA AND POWER ANALYSIS WITH D-LATCH ENABLED CARRY SELECT ADDER USING GATE DIFFUSION INPUT

SAKSHI BHATNAGAR[1] and VIMAL AGRAWAL[2]

ABSTRACT- Arithmetic operation addition is the most frequently used in micro-processors, signal processors of digital computers. It acts as a back bone for the combination of other arithmetic operations like subtraction, multiplication. Therefore, for the proficient   execution of any arithmetic unit, the adder configuration has become an important hardware unit. There exists a vast variety of circuit architectures with different parameters and performance characteristics which are widely used in the practice. VLSI designs require compact area and low power systems. The overall area reduction of the system is decided at all the level of its architecture, fabrication designs, logic gates design, optimization of circuits, gate clocking , layout etc. In this paper, Carry   select adders are implemented using BEC-1 and D-Latch with Gate Diffusion Input (GDI) using TANNER software tool and are compared in terms of Area and Power Utilization.

I.   INTRODUCTION

Various adders have been used in day to day lifestyle. Adders are used mainly in arithmetic devices where calculations are mainly used. Thus, adders are the most significant part of VLSI chip designing systems. Here, in this paper, carry select adder has been structured in two ways, first by using BEC-1 and second by using D- Latch with Gate Diffusion Input (GDI). Then using Tanner tool v13.0, the two structures are executed. Section II contains the detail of Carry Select Adder using BEC-1 and D-Latch enabled CSA and their Tanner implementation. Section III contains the result of the work done and section IV concludes that which adder is much more efficient than other.

II.   IMPLEMENTATION OF CSA

VLSI designs require compact and low power systems, components that dissipate and consume low power. Small size of the circuits not only provides reduced power consumption but it also provides faster speed to the overall system. Modern portable battery operated devices such as cell phones, laptops; PDAs are particularly affected by high power dissipation as it reduces battery service life. Thus power dissipation has now become a vital design metric. When we use any digital device, we want high performance rate, however, we can't always get the output with full swing mainly due to dissipation of power in the circuits. Switching frequency, load capacitance can be the reasons for

[1] *Apex Institute of Engineering and Technology, Jaipur, India*

[2] *Apex Institute of Engineering and Technology, Jaipur, India*

dissipation of power. This leakage power dissipated during sleep/standby mode of any device is given by:

PLEAK = ILEAK * VDD

To reduce the consumption of power, Carry Select Adder has been structured using BEC-1 rather than ripple carry adder as BEC-1 contains less quantity of MOSFETs. Ripple carry adder and internal structure of BEC-1 are shown in figure 1 and figure 2 respectively.
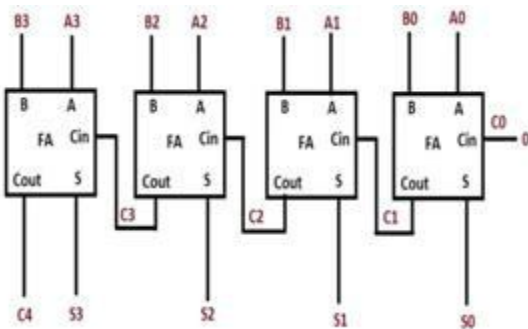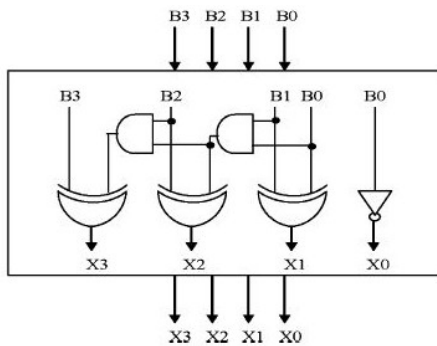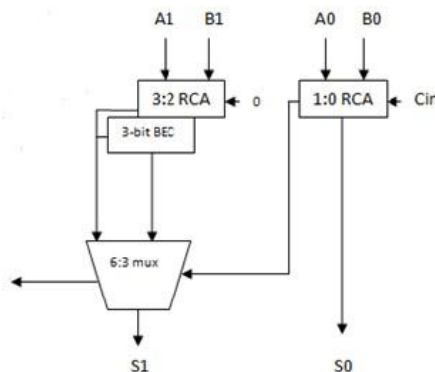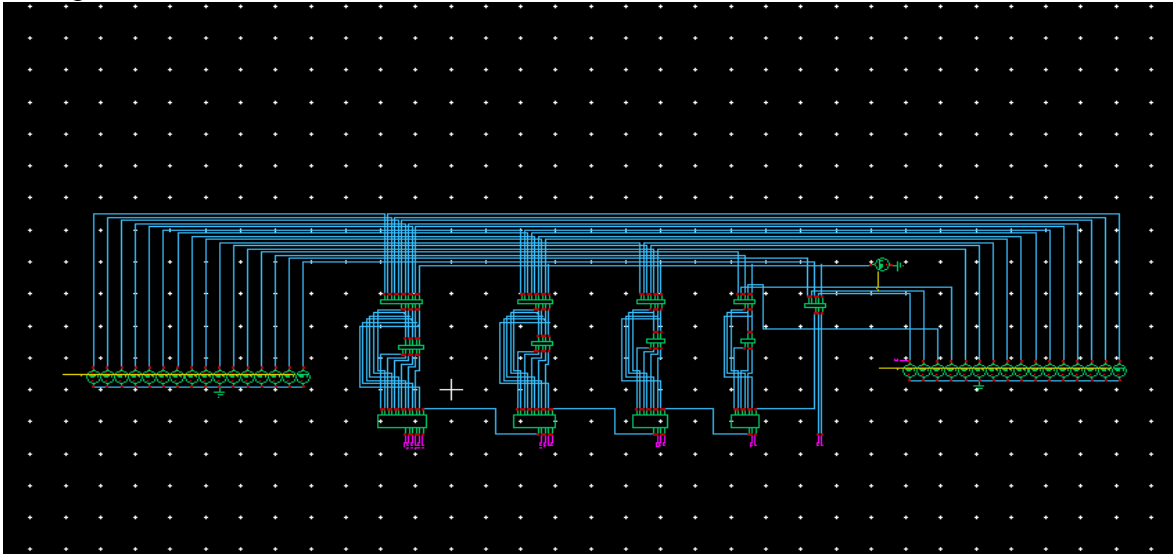
Figure 1: Ripple Carry Adder

Figure 2: Internal circuit of BEC-1

It can be clearly seen from the figures 1 & 2 that MOSFET counts in RCA is more as compared to BEC-1. Therefore, in regular CSA one of the two ripple carry adders are first replaced by BEC-1 to decrease the count of MOSFETs which is shown in figure 3:
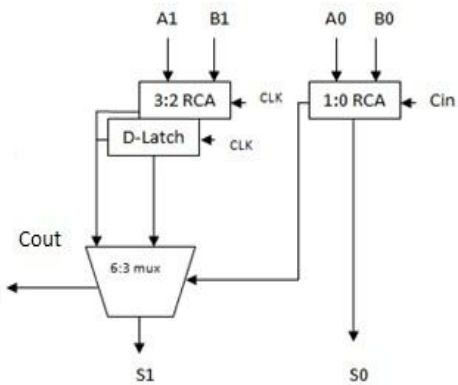
Figure 3: 2-bit BEC-1 Enabled CSA Implementation of the above mentioned figure has been done through Tanner tool.
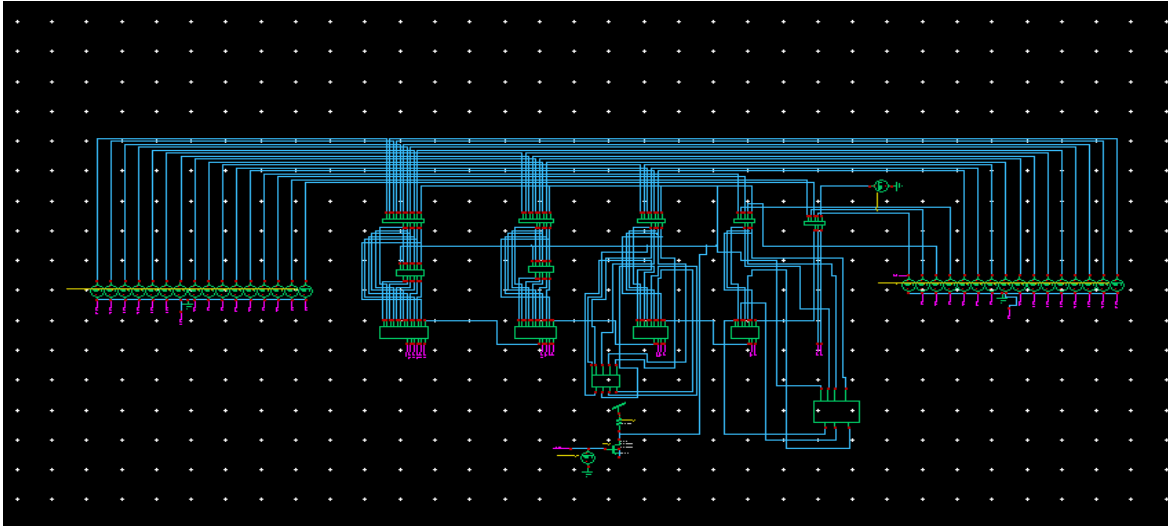

Figure 4: Implementation of BEC-1 Enabled CSA

Now further, BEC-1 is replaced by D-Latch with Gate Diffusion Input (GDI). D-Latch acts as a storage device for 1- bit data. Regular CSA now consist of one ripple carry adder and a D-Latch in its one group of the circuit.

Figure 5: 2-bit D-Latch enabled CSA Implementation of the above mentioned figure has been done through Tanner tool.

Figure 6: Implementation of D-Latch with Gate Diffusion Input (GDI) enabled CSA

During switching time period, PMOS and NMOS transistors in any CMOS device conduct current for the period of one-half each. Average power consumption of CMOS can be given by:

$$PAvg = \alpha.Cload.V^2DD.f$$

Where,

α denotes switching activity factor, C_L denotes load capacitance. V_{DD} represents supply voltage, f is the operating frequency

Data dependent function of switching activity is power dissipation. Switching power can be reduced by following:

i)   Reducing the supply voltage

ii)   Reducing operating frequency

iii)   Reducing the switching activity of effective load capacitance [2].

Effective capacitance C_{eff} of switching operations is the multiplication of load capacitance and switching factor i.e.

$$Ceff = CL * \alpha$$

Switching activity must be appropriately evaluated in order to estimate the energy consumption of the adders. By estimating the accurate switching activity of the adders, accurate switching power can be detected.

III.   RESULTS

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Implemented CSAs are much more efficient than regular CSA. The waveform of the implemented CSA has been shown below in figure 7:
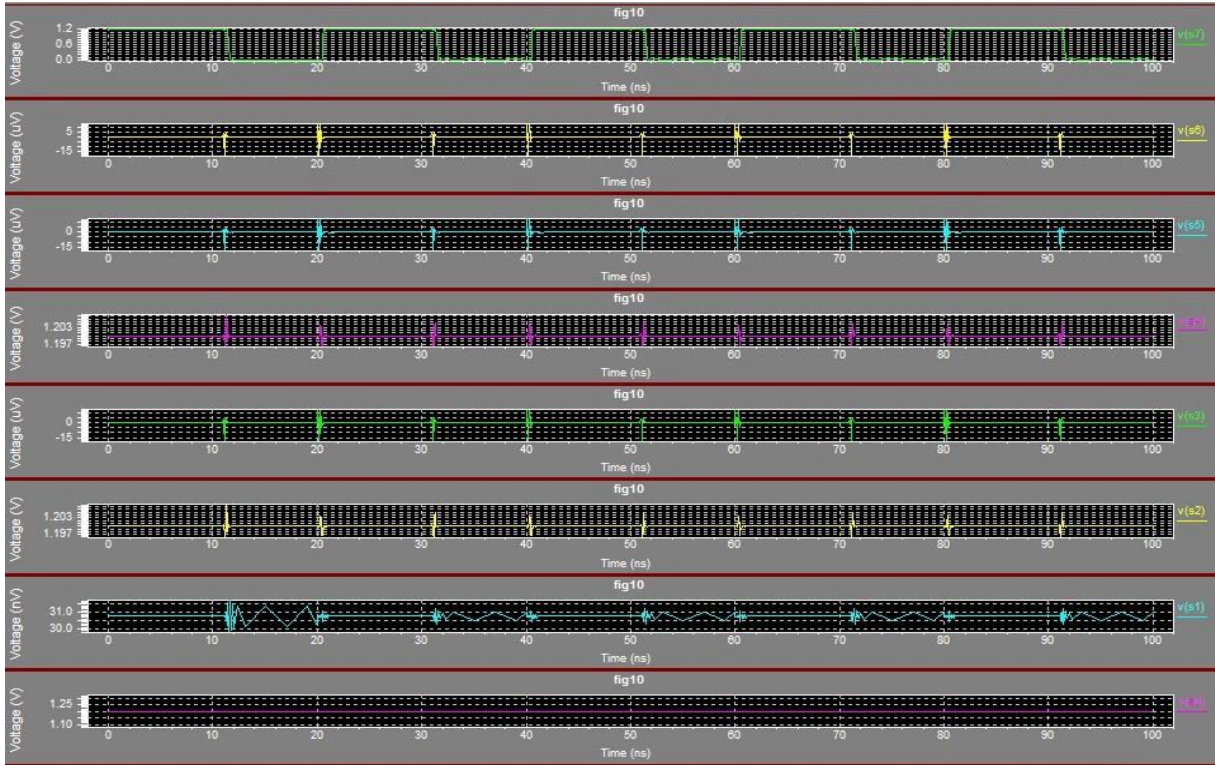
Figure 8: Waveform of implemented CSA

According to the calculation and analysis done for MOSFET counts as well as power consumption by the implementation of CSAs using BEC-1 and D-Latch, it has been analyzed that CSA using BEC-1 as a replacement for ripple carry adder is much more efficient than CSA using D-Latch as a replacement in terms of power consumption..

However, D-Latch with Gate Diffusion Input (GDI) is more efficient in terms of MOSFETs Count when compared with BEC-1 Enabled CSA which contains only 936 MOSFETs. CSA with Bec-1 has more number of MOSFETs which makes it bulkier than D-Latch with Gate Diffusion Input (GDI). Table showing comparison of gate counts and consumption with their graphical representation are as follows:

TABLE 1: Number of MOSFETs and Consumption of Power of Implemented Adders

S.No.	Carry Select Adder	MOSFET Counts	Power Consumption (Watts)

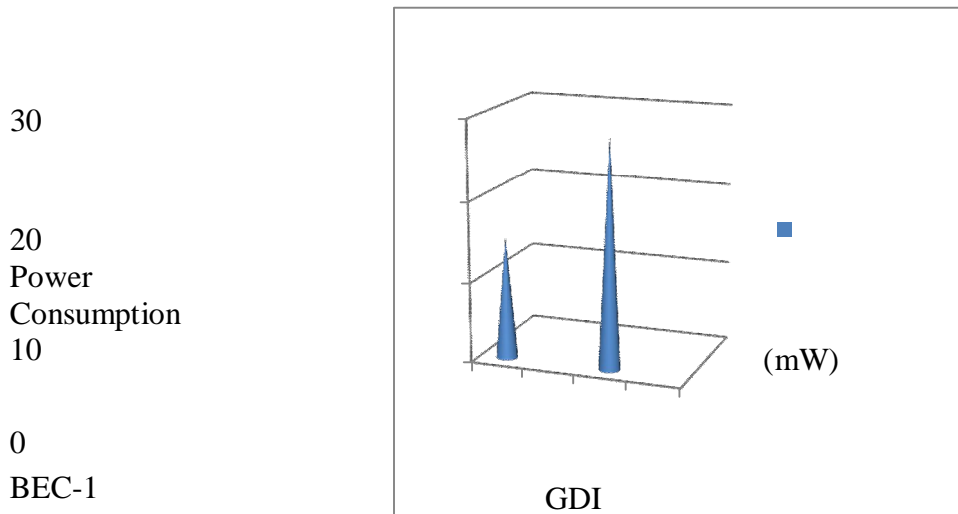|			
1.	BEC-1 enabled	1288	1.527126 e-002
2.	D-Latch with GDI enabled	936	2.851438 e-002
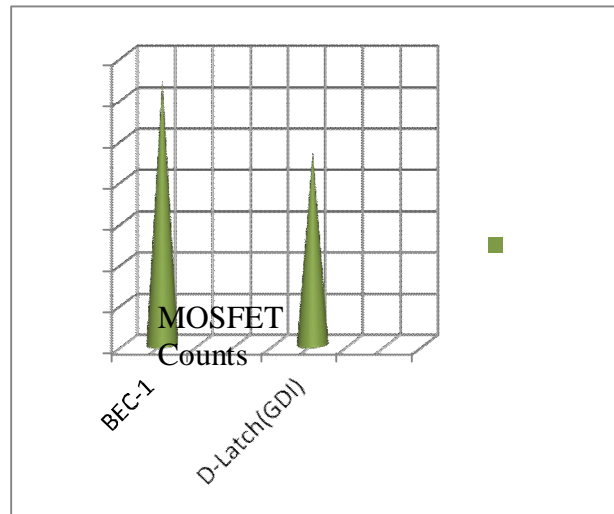
Figure 9: Comparison of MOSFETs between BEC-1 and D-Latch (GDI) enabled CSA

From graphical representation above, it can be seen evidently that D-Latch with GDI enabled CSA.is more area efficient when compared with BEC-1 enabled CSA.

Now, the power consumption of BEC-1 enabled CSA and D-Latch with GDI enabled CSA has been compared graphically which is represented below in figure 10.

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30

20
Power
Consumption
10

0
BEC-1

GDI

(mW)

Figure 10: Comparison of Power Consumption between BEC-1 and D-Latch (GDI) enabled CSA

From graphical representation above, it can be seen evidently that D-Latch with GDI enabled CSA has more power consumption when compared to BEC-1 enabled CSA.

IV.   CONCLUSION

According to the analysis done through Tanner tool, it can be concluded that BEC-1 enabled CSA has 352 MOSFETs more than D-Latch with GDI enabled CSA, while having less consumption of power. According to the analysis and calculations it can be said that D-Latch with GDI enabled CSA is more area efficient than BEC-1 enabled CSA. However, it is less efficient in terms of consumption of power.

V.   REFERENCES

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