

Implementation Full Bridge Series Resonant Buck Boost Inverter

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Abstract: Voltage-source PWM inverters have been widely used in industrial applications such as uninterruptible power supplies, static frequency changers and variable speed drives. This is due to their capability in allowing continuous and linear control of the frequency and fundamental component of the output voltage. However, the conventional voltage source inverter (VSI), referred to as buck inverter in this paper, is probably the most popular and important power converter topology. One of the characteristics of the buck inverter is that the instantaneous average output voltage is always lower than the input dc voltage. As a consequence, when an output voltage larger than the input is needed, a boost converter must be used between the dc source and the inverter. Depending on the power and voltage levels involved, this solution can result in high volume, weight, cost and reduced efficiency. Recent years have seen development of numerous PWM pattern generation techniques for improving the performance of a voltage source inverter. They can be divided into forward PWM techniques and real time wave form feedback control techniques. But, these PWM techniques are based on the assumption of an ideal input dc voltage which is achieved by using a dc link filter with bulky inductor capacitor components. This, however increases the cost and size, and reduces the overall efficiency. Besides, due to a large step change in input dc voltage for instance, a transient overshoot may be observed at the output end. Thus, lots of elapsed control cycles are required to settle the system operation. In this paper, a novel single-stage full-bridge series-resonant buck-boost inverter (FB-SRBBI) is proposed, which naturally generates an output ac voltage lower or larger than the input dc voltage depending on the duty-cycle. The inverter only includes a conventional full-bridge topology and a LC resonant tank without auxiliary switches. Thus, its configuration is inherently simple and compact. The nonlinear control strategy is designed against the input dc perturbation and achieves good dynamic regulation and properly gates the power switches and building resonance in the LC tank is proposed. [1]

Keywords: zero voltage switching, zerocurrent switching, parallel resonant DC-Link

I. INTRODUCTION

In the conventional dc-ac power conversion field, the input to the voltage source PWM inverters is a stiff dc voltage supply. Because the inverter switches operate in a switch mode, the inverter switching devices are subjected to very high switching stresses and switching power losses that increase linearly with the switching frequency of the pulse-width-modulation. As a consequence, the switching frequencies of commercially available medium to high power range transistorized PWM inverters in ac machine drive and uninterruptible-power-supply (UPS) applications are limited to utmost a few kHz, even though higher switching frequencies are greatly desired to yield a higher system performance and a lower acoustic noise. Recently, remarkable efforts have been made in the development of high-frequency zero-voltage-switching (ZVS) and zero-current switching (ZCS) dc-ac power inverters due to the increasing demand of high switching frequency dc-ac inverters which are able to realize highly dynamic, high performance and negligible noise ac machine drive systems as well as UPS systems. Various ZVS and/or ZCS dc-ac inverter topologies have been proposed and reported. As a viable approach to obtain ZVS high switching frequency power inverters, the Parallel-Resonant DC-Link (PRDCL) circuit was proposed.

The proposed PRDCL circuit is aimed at both providing short zero voltage intervals in the dc link of the PWM inverter during the required inverter device switching transition periods and imposing minimum voltage stresses on the inverter devices. Because of the ZVS nature, the proposed PRDCL inverter system can be efficiently operated at very high switching frequencies with a minimum peak dc bus voltage stress. In fact, the peak dc link voltage is equal to the dc supply voltage V . Moreover, the conventional PWM strategy, which is very simple and widely used in industry, can still be used for controlling the ZVS inverter. Additionally, the resonant tank circuit in

this topology is minimally involved in the system power transfer, which is very much desired. The recent development of the PRDCL circuit which includes the circuit control scheme, system implementation the power semiconductor device evaluations are also provided. This paper concludes with a comparison of the new PRDCL PWM inverter system with the conventional

voltage source PWM inverter on the basis of the parameters considered important in determining the applicability of the proposed system for dc-ac power conversion applications. (3) The uninterrupted power supply (UPS) has been important equipment for electronic apparatus. The phase-controlled (PC) and pulse-width-modulated (PWM) techniques have been well developed for realizing the usual UPS. Due to high stress, high switching loss, and large EMI in the usual PWM converter and inverter, the zero-current switching (ZCS) and zero-voltage switching (ZVS) are explored. However, the power switches still operate in pulsed fluctuation in either voltage or current switching, which results in high di/dt and dv/dt and significantly limits the inverter or converter to operate at high frequency. The purpose of this study of series resonant dc/ac inverter is to achieve an ac sinusoidal waveform synthesized by a series of quasi sinusoidal pulses (QSP's) that are formed by series resonance.

Each QSP generated from the resonant tank is energized by the power switch, which is driven by a modulated duty rate and operates in the forced discontinuous-conduction mode (FDCM). The FDCM is named due to the cease conduction of the power switch, which can be made by the desired duty rate of the control pulses during the series-resonant action. No square-pulsed voltage or current waveform will occur on the power switch during the switching period. The power switch features turn-on at zero-current and low finite-voltage switching and turn-off at low finite-current and lower finite voltage switching. Thus, the power switch is capable of low voltage and current stresses, low switching loss, and low EMI. The pulse train with modulated duty rate for driving the power switch is provided by a modified PWM (M-PWM) controller. The controller consists of a triangular waveform generator (TWG), a sinusoidal waveform generator (SWG), and some logic gates. The M-PWM controller is inherently a voltage-controlled modulator and its frequency is certainly the switching frequency. The duty rate of the driving pulse is not greater than 50% of the switching period and varies in proportion to the amplitude of the sinusoidal waveform. (4)

Sinusoidal Pulse Width Modulation

The switches in the voltage source inverter (See Fig.1.1) can be turned on and off as required. In the simplest approach, the top switch is turned on. If turned on and off only once in each cycle, a square wave waveform results. However, if turned on several times in a cycle an improved harmonic profile may be achieved.

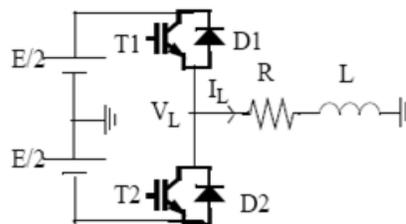


Fig 1.1 simple voltage sourced inverter

In the most straight forward implementation, generation of the desired output voltage is achieved comparing the desired reference waveform (modulating signal) with a high-frequency triangular 'carrier' wave as depicted schematically in Fig 1.2. Depending on whether the signal voltage is larger or smaller than the carrier waveform, either the positive or negative dc bus voltage is applied at the output. It may be noted that over the period of one triangular wave, the average voltage applied to the load is proportional to the amplitude of the signal (assumed constant) during this period.

The resulting chopped square waveform contains a replica of the desired waveform in its low frequency components, with the higher frequency components being at frequencies close to the carrier frequency. Notice that the root mean square value of the ac voltage waveform is still equal to the dc bus voltage, and hence the

total harmonic distortion is not affected by the PWM process. The harmonic components are merely shifted into the higher frequency range and are automatically filtered due to inductances in the ac system.

When the modulating signal is a sinusoid of amplitude A_m , and the amplitude of the triangular carrier is A_c , the ratio $m=A_m/A_c$ is known as the modulation index. Note that controlling the modulation index therefore controls the amplitude of the applied output voltage. With a sufficiently high carrier frequency (see Fig 1. 3 drawn for $f_c/f_m = 48$ and $t = L/R = T/3$; $T =$ period of fundamental), the high frequency components do not propagate significantly in the ac network (or load) due the presence of the inductive elements. However, a higher carrier frequency does result in a larger number of switching's per cycle and hence in an increased power loss. Typically switching frequencies in the 2-15 kHz range are considered adequate for power systems applications. Also in three-phase systems it is advisable to use $f_c / f_m=3k$ ($k=n$) so that all three waveforms are symmetrical.

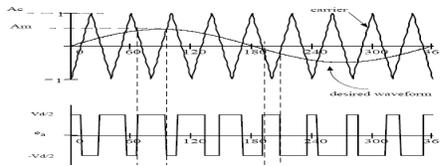


Fig 1.2: Principle of Pulse Width Modulation

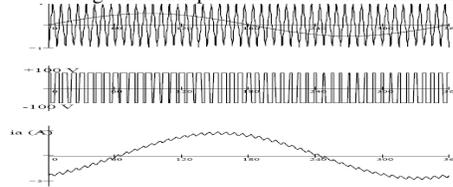


Fig.1.3: SPWM with $f_c/f_m = 48$, $L/R = T/3$

Note that the process works well for $M < 1$. For $M > 1$, there are periods of the triangular wave in which there is no intersection of the carrier and the signal. However, a certain amount of this “over modulation” is often allowed in the interest of obtaining a larger ac voltage magnitude even though the spectral content of the voltage is rendered somewhat poorer. Note that with an odd ratio for f_c/f_m , the waveform is anti-symmetric over a 360 degree cycle. With an even number, there are harmonics of even order, but in particular also a small dc component. Hence an even number is not recommended for single phase inverters, particularly for small ratios of f_c/f_m .

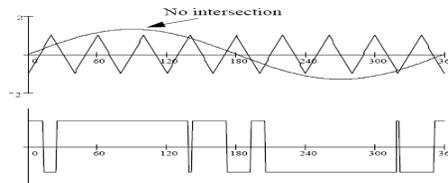


Fig 1.4 Over modulation $M=1.3$

II. SIMULATION

2.1 Simulation Diagram:

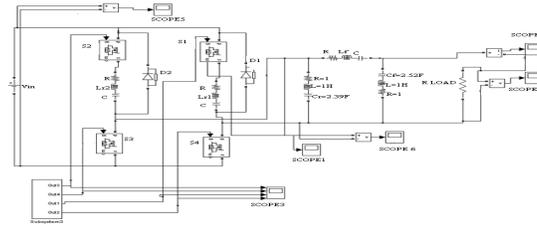


Fig 2.1(a) diagram of power circuit

2.2 Sub System

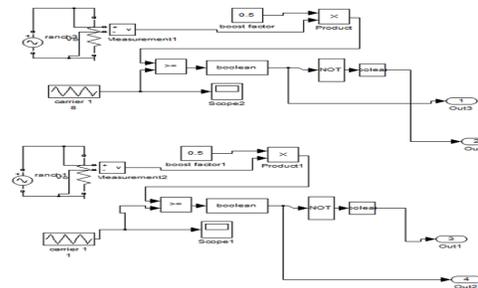


Fig 2.2(a) Subsystem for Power circuit to trigger the MOSFET by PWM pulses

By PWM technique generating sine shape and comparing with switching frequency of triangular wave and generating PWM with that PWM pulse will converting into four PWM then switching the switches alternatively.

2.3 Simulation Results

Input Voltage 10 V

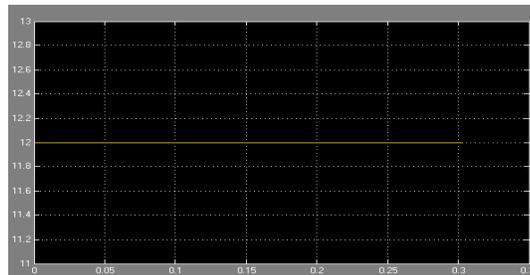


Fig 2.3(a) input Voltage

Boosted Voltage 12 V

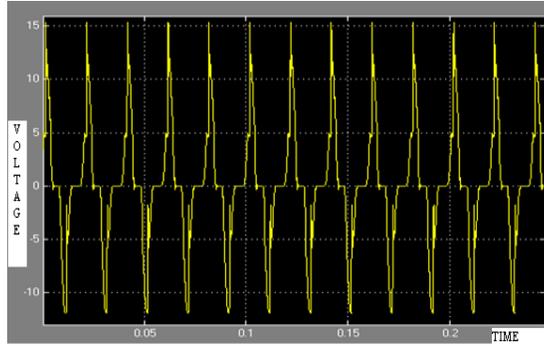


Fig 2.3(b) Boosted Voltage Waveform

Boost output current

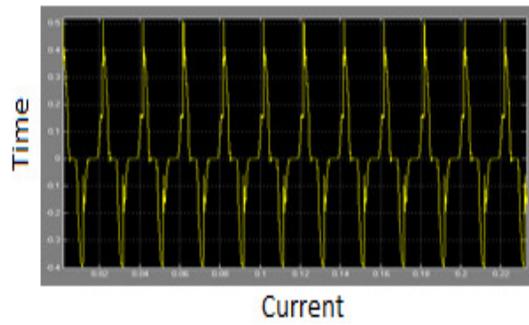


Fig 2.3(c) Boosted Current Waveform

a) Buck output Voltage

a) Output voltage 2 V

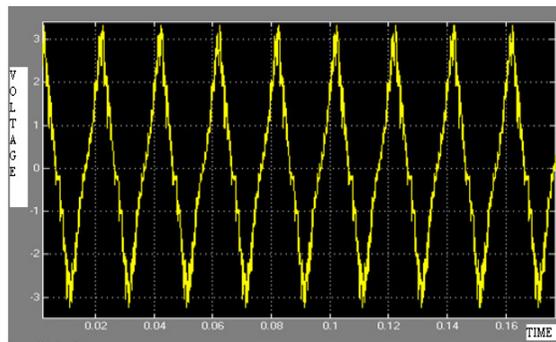


Fig 2.3(d) Buck Voltage waveform

b) Buck output current

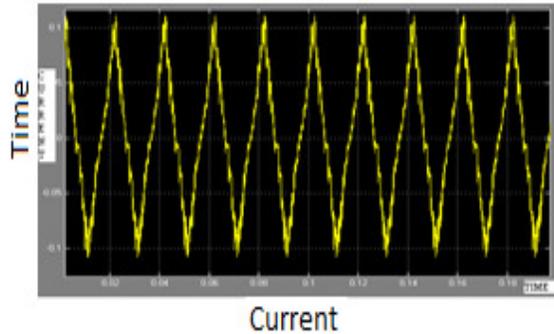


Fig 2.3(e) Buck current waveform

III. CONCLUSION

A single-stage FB-SRBBI is presented with simple and compact configuration. The proposed inverter is applicable in UPS design, whenever an ac output voltage larger than the dc link voltage is needed, with no need of a second power conversion stage. The active switches are operated at a fixed frequency with the pulse width modulation technique. A resonant cell is built in the power stage to build ZCS for turning on the power switches. In this paper, an attempt has been made and succeeded to overcome the losses occurred due to harmonics in a conventional inverter. This full bridge series resonant buck boost inverter has significant advantage over the conventional one because this can operate at nearly sinusoidal current waveform and higher output voltage.

The full bridge series resonant buck boost inverter has a power transfer of four times and voltage twice that of half bridge series resonant buck boost inverter. The performance of the inverter has been checked through both simulation and experimental studies and found to be satisfactory.

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